2012

ANNUAL INTERNATIONAL COURSES IN

TELECOMMUNICATIONS
SEMICONDUCTOR TECHNOLOGY
NANOTECHNOLOGY

Signal Integrity: Advanced High-Speed Design and Characterization

Dr. István Novák
Oracle, MA, USA

CEI-Europe Advanced Technology Education
CONTINUING EDUCATION INSTITUTE - EUROPE

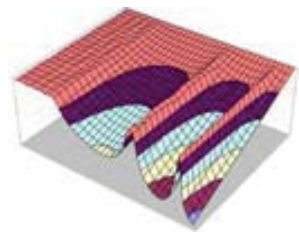
www.cei.se

CEI-Europe • Linköping • Sweden • Ph +46 13 100 730 • Fax +46 13 100 731 • cei@cei.se • www.cei.se

A few representative slides from:

Signal Integrity: Advanced High-Speed Design and Characterization

CEI course #55



István Novák, Ph.D.

Oracle
Boston, MA, USA

http://www.electrical-integrity.com

Table of Contents

Illustration files are distributed separately

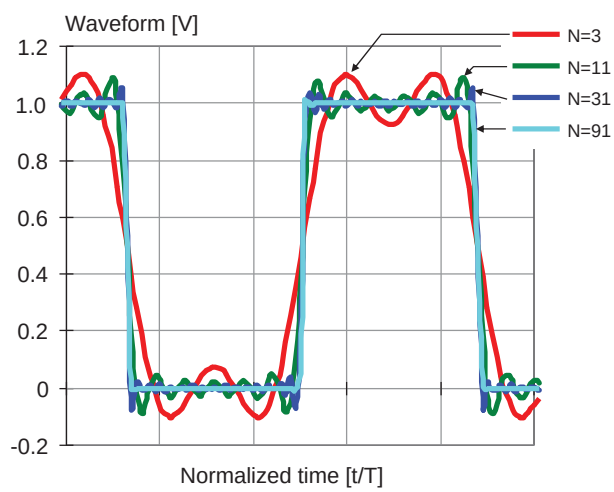
When Signal and Power Integrity Fails

NOAA satellite imagery one day before and the night of the 2003 North American blackout.

Source:http://en.wikipedia.org/wiki/2003_North_America_blackout
http://en.wikipedia.org/wiki/NOAA

istvan.novak@ieee.org
www.electrical-integrity.com

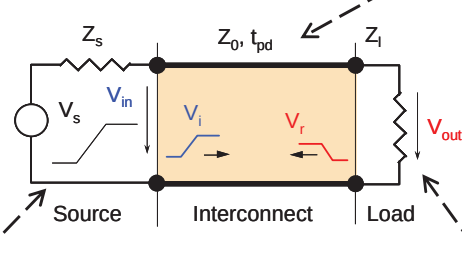
Harmonic Composition



f_0 = 10MHz
D = 50 %
t_r = 1 nsec
t_f = 1 nsec

istvan.novak@ieee.org
www.electrical-integrity.com

Distortions in Digital Interconnection



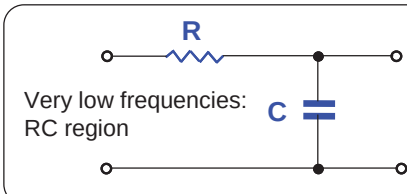
Interconnects:
* Reflections
* Stub ringing
* Crosstalk
* Simultaneous switching
* Losses, dispersion

Driver:
* Power-supply noise
* Simultaneous Switching
* Crosstalk in Package

Receiver:
* Reflections
* Simultaneous Switching
* Power-supply noise
* Self oscillation

istvan.novak@ieee.org
www.electrical-integrity.com

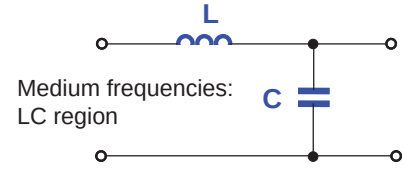
Transmission Line Performance
RC and LC Delay Regions



Very low frequencies:
RC region

$$\omega L << R$$

$$Z_0 = \sqrt{\frac{R}{j\omega C}} \qquad t_{pd} = RC$$



Medium frequencies:
LC region

$$\omega L >> R, \quad \omega C >> G$$

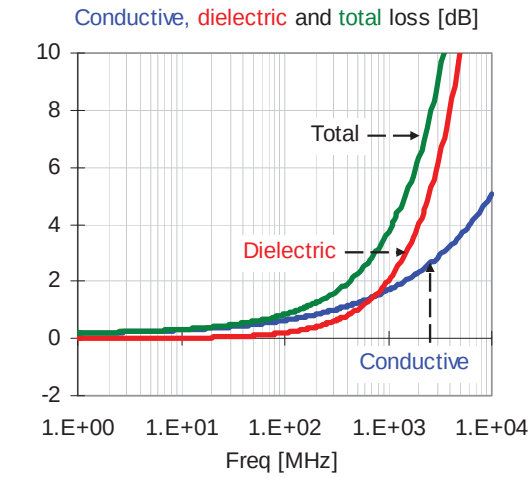
$$Z_0 = \sqrt{\frac{L}{C}} \qquad t_{pd} = \sqrt{LC}$$

H. Johnson, M. Graham:High Speed Signal Propagation, Prentice Hall, NJ, 2003, p.148-184

istvan.novak@ieee.org
www.electrical-integrity.com

Transmission Line Performance

Skin and Dielectric Loss Regions



- 50-ohm matched trace
- FR4 ($\tan\delta = 0.02$)
- w = 0.2 mm (8 mils)
- length = 43cm (17")

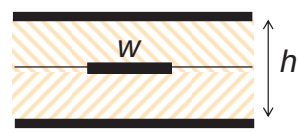
H. Johnson, M. Graham:High Speed Signal Propagation, Prentice Hall, NJ, 2003, p.121

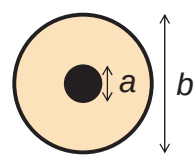
istvan.novak@ieee.org
www.electrical-integrity.com

Transmission Lines: Scaling Rules

For a given material, assuming thin conductor:

- t_{pd} depends on length and propagation medium (ε_{eff}), but not on cross section
- Z_0 depends only on proportions (w/h, b/a)





istvan.novak@ieee.org
www.electrical-integrity.com

When to Worry About Reflections
Allowable mismatch

Consider terminations whenever in a high-speed system the passive propagation delay is a non-negligible fraction of rise/fall times

Safe limit rule to ignore terminations:

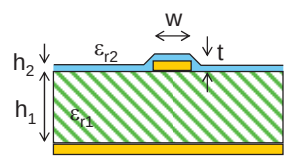
$2t_{pd} < 0.1t_r$

Tight matching makes sense only on medium-speed point-to-point interconnects

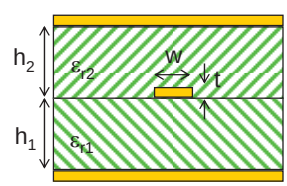
istvan.novak@ieee.org
www.electrical-integrity.com

Impedance Accuracy

* Surface microstrip (+/-15% typical)
  - Dielectric heights (h_1, h_2)
  - Trace cross section dimensions (w, t)
  - Dielectric constants (ε_{r1}, ε_{r2})
  - Plating
  - Cover layer
  - SSN/Xtk
  - Proximity effects (voids, nearby objects)

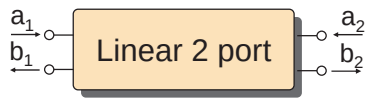


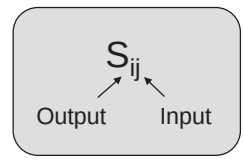
* Stripline (+/-10% typical)
  - Dielectric heights (h_1, h_2)
  - Trace cross section dimensions (w, t)
  - Dielectric constants (ε_{r1}, ε_{r2})
  - SSN/Xtk
  - Proximity effects (voids, nearby objects)



istvan.novak@ieee.org
www.electrical-integrity.com

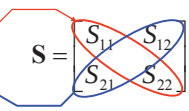
S Parameters
Physical Meaning





$$S_{11}=\left.\frac{b_1}{a_1}\right|_{a_2=0} \quad S_{22}=\left.\frac{b_2}{a_2}\right|_{a_1=0} \quad S_{21}=\left.\frac{b_2}{a_1}\right|_{a_2=0} \quad S_{12}=\left.\frac{b_1}{a_2}\right|_{a_1=0}$$

- Matched termination is assumed on all ports
- Matching is with an arbitrary reference impedance
- Main diagonal elements (S_{ii}): reflections
- Off-diagonal elements (Sij): wave transmissions



istvan.novak@ieee.org
www.electrical-integrity.com

Reflection Loss
Insertion Loss

Reflection Loss: (Return Loss)

$$RL=-20\log|\Gamma|dB$$

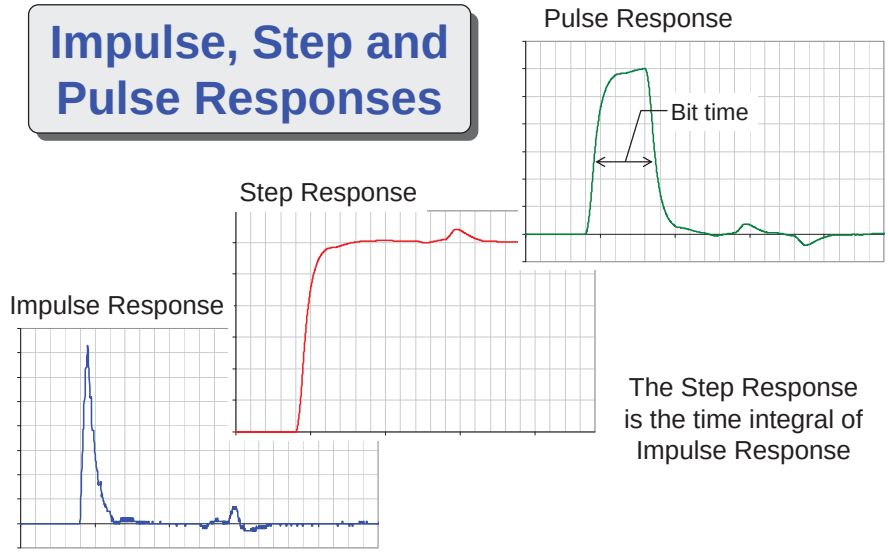
$$\text{Insertion Loss} = \frac{\text{Power delivered to the load without the two port}}{\text{Power delivered to the load with the two port}}$$

$$IL=\frac{|(1-S_{11}\Gamma_s)(1-S_{22}\Gamma_L)-S_{12}S_{21}\Gamma_S\Gamma_L|^2}{|S_{21}|^2(1-|\Gamma_S\Gamma_L|^2)}=\frac{1}{|S_{21}|^2}\text{ if no reflection}$$

David M. Pozar: Microwave Engineering, Wiley, 2005, p.59
Besser-Gilmore: Practical RF Circuit Design, Artech House, 2003, p. 195

istvan.novak@ieee.org
www.electrical-integrity.com

Impulse, Step and Pulse Responses

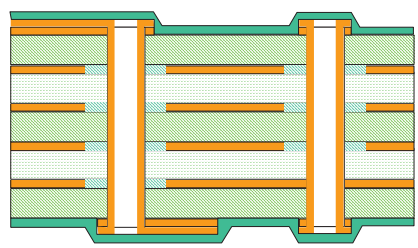


The Step Response is the time integral of Impulse Response

istvan.novak@ieee.org
www.electrical-integrity.com

Regular Rigid Board Process

* Lowest cost:
  - Foil construction
  - Symmetrical stackup
  - Through-holes only
* Pattern inner layer cores
* Press
* Drill
* Etch outer layers
* Plate
* Finish



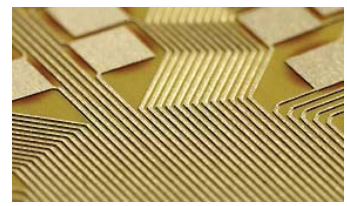
istvan.novak@ieee.org
www.electrical-integrity.com

Process Impact on SI

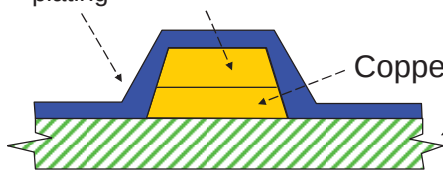
For trace width and plane thickness:

* Most accurate are unplated inner layers
* Plated inner layers are less accurate
* Least accurate are plated outer layers due to solder mask and plating

35/35 μm trace from Cicorel

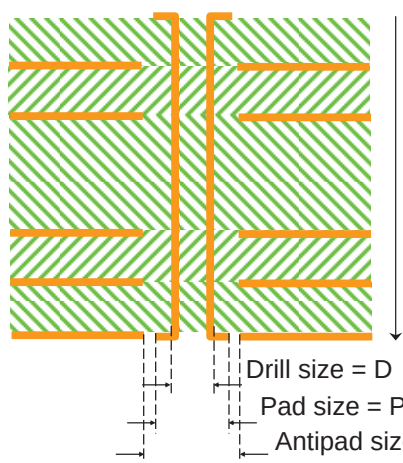


Source: http://www.aerospace-technology.com



istvan.novak@ieee.org
www.electrical-integrity.com

Via Dimensions



Typical geometry:

L: up to several mm

D_{min} = 0.25 mm

P = D_{min} + 0.25 mm

A = D_{min} + 0.5 mm

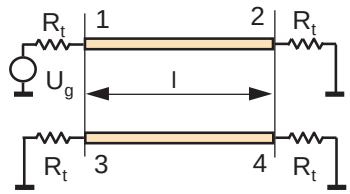
L/D < 10

istvan.novak@ieee.org
www.electrical-integrity.com

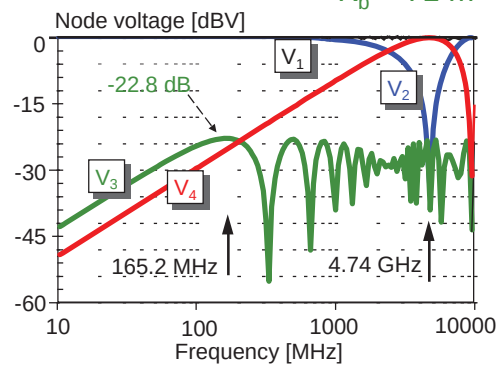
Crosstalk in Matched Microstrip

Simulated output:
C = 2.3 pF, C_M = 88 fF,
L = 10 nH, L_M = 1 nH
K_b = 71 m

Input data:

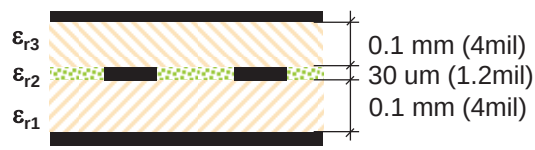


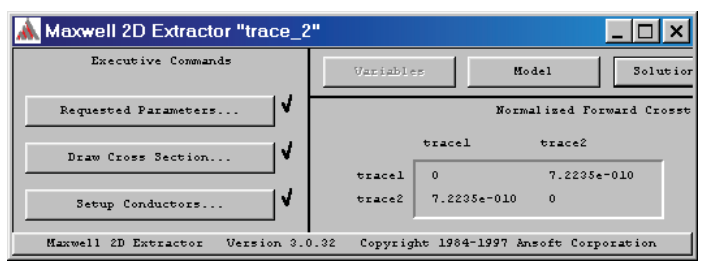
Surface microstrip
w/h = 1, s/h = 2
l = 25.4 cm (10 inch)
ε_r = 4.7
$Z_0 = R_t$ = 65.7 ohms
Ug = 1 V



istvan.novak@ieee.org
www.electrical-integrity.com

Non-homogeneity in Stripline

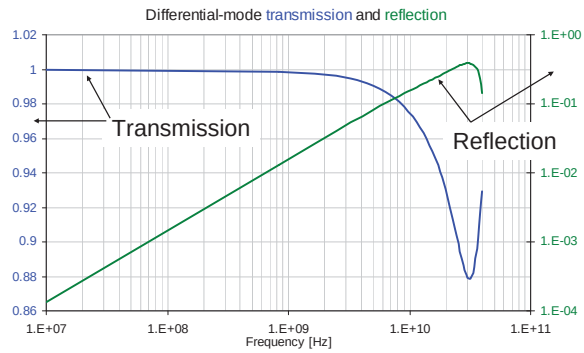


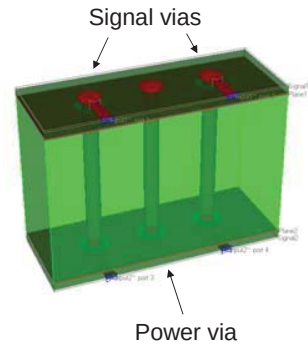


istvan.novak@ieee.org
www.electrical-integrity.com

Resonance Crosstalk

Any (unrelated) resonating structure can increase coupling between aggressor and victim

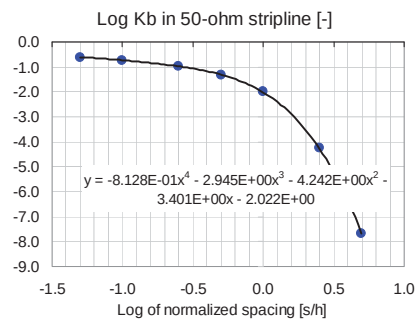


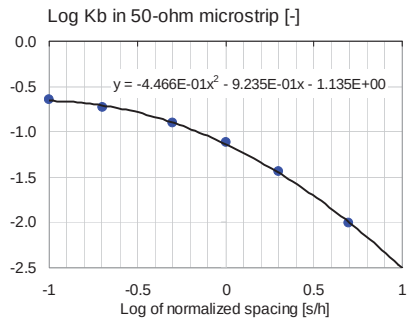


Simulated with Simbeor

istvan.novak@ieee.org
www.electrical-integrity.com

Decay of Crosstalk with Distance





* In stripline, K_b drops with the fourth power of distance
* In microstrip, K_b drops with the second power of distance

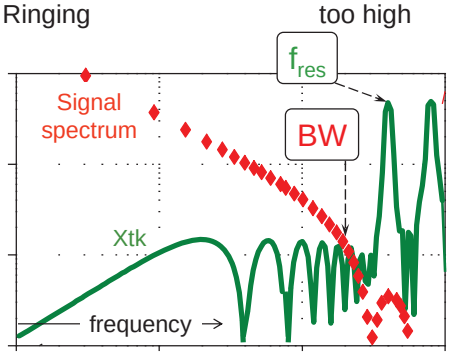
istvan.novak@ieee.org
www.electrical-integrity.com

Shield Conductor, Design Rules

Signal rise time t_r	1nsec	3nsec
Signal bandwidth BW	286 MHz	86 MHz
Lowest resonance f_{res}	340 MHz	340 MHz
Ringing	too high	acceptable

$$f_{res} = \frac{c}{2l\sqrt{\varepsilon_r}}$$

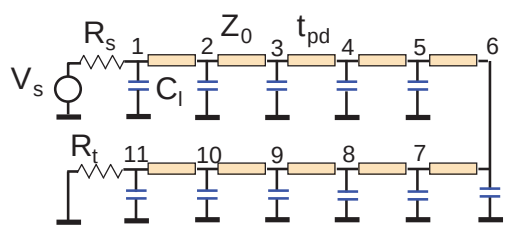
$$BW = \frac{0.35}{t_r}$$



Approximate rule:
$2t_{pd} < t_r$

istvan.novak@ieee.org
www.electrical-integrity.com

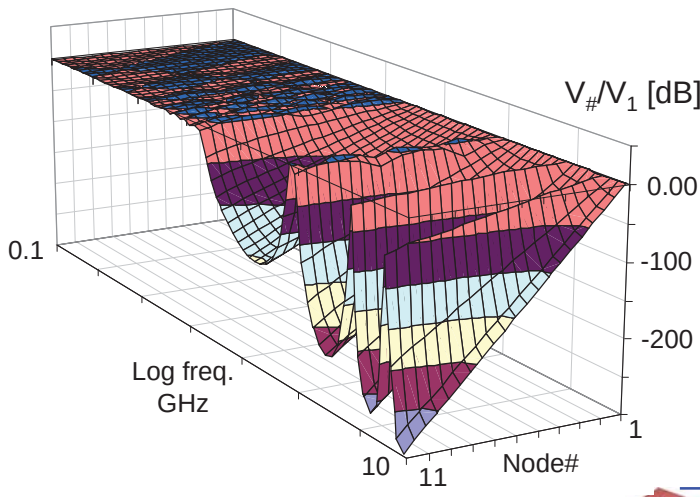
Multiple Loads Along Interconnect



- 10 segments of transmission lines, 11 load capacitors
- For all segments: Z_0 = 50 ohms, t_{pd} = 0.18 nsec (2.5 cm ~ 1")
- V_s: piece-wise linear 0.5 to 3.5 V step, R_s ~ 0.

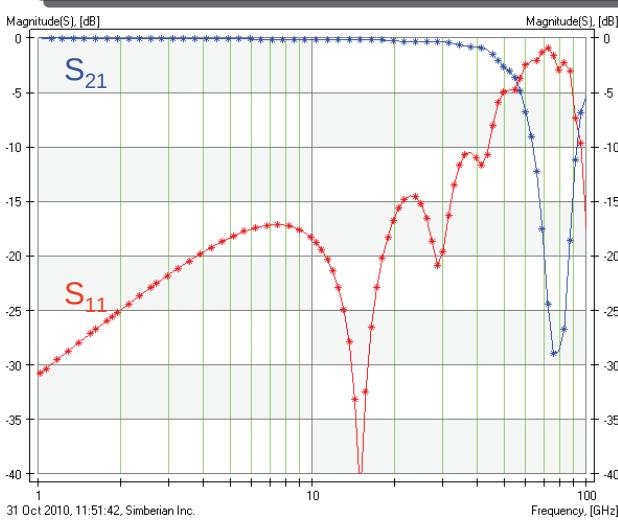
istvan.novak@ieee.org
www.electrical-integrity.com

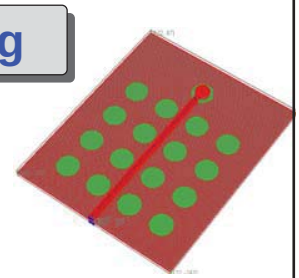
The Loaded Line is a Filter!



istvan.novak@ieee.org
www.electrical-integrity.com

Plane Perforation Loading





Plane perforations change trace impedance

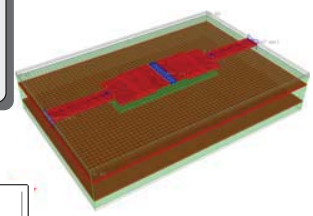
Periodical perforations filter signals

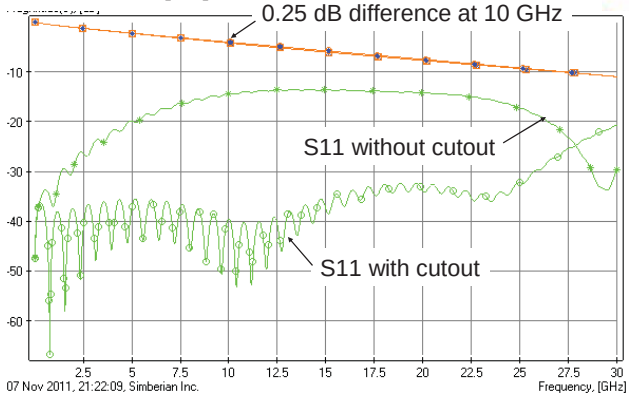
Simulated with Simbeor

Attenuation in PCB Traces Due to Periodical Discontinuities, DesignCon 2006, February 6-9, 2006, Santa Clara, CA

istvan.novak@ieee.org
www.electrical-integrity.com

Optimizing DC Blocking Capacitors



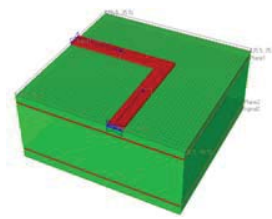


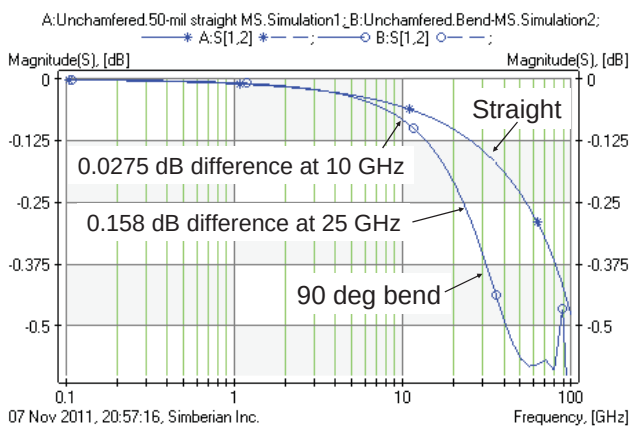
- 8-mil trace
- FR4 dielectric
- 0402 capacitor
- 20x60mil optional cutout on plane

Simulated with Simbeor

istvan.novak@ieee.org
www.electrical-integrity.com

90 Degree Bends





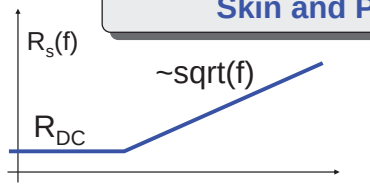
- 6-mil trace
- FR4 dielectric
- No chamfer

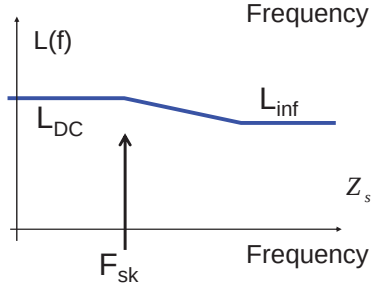
Simulated with Simbeor

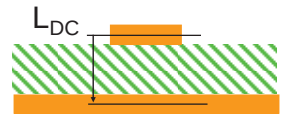
istvan.novak@ieee.org
www.electrical-integrity.com

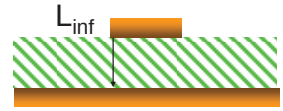
Inductance vs. Resistance

Skin and Proximity Effects









$$Z_s(f) = (1-j)R_{RF}\sqrt{f}\cot\left((1-j)\frac{R_{RF}}{R_{DC}}\sqrt{f}\right)$$

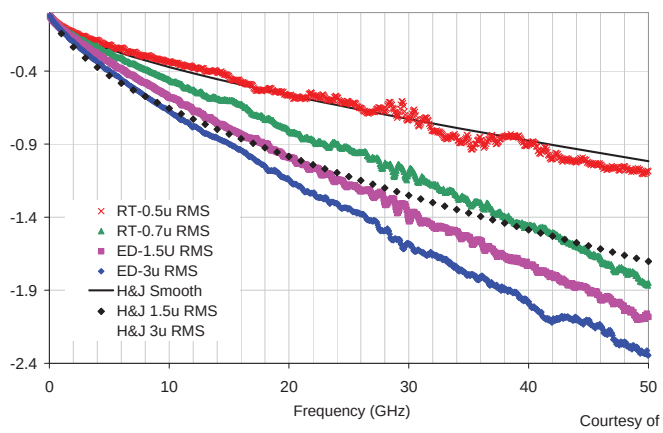
$$R_{DC} = \frac{1}{\sigma t} \qquad R_{RF} = \sqrt{\frac{\pi\mu}{\sigma}}$$

J.C. Rautio, V. Demir, "Microstrip Conductor Loss Models for Electromagnetic Analysis," IEEE Tr. MTT, March 2003, p.915

istvan.novak@ieee.org
www.electrical-integrity.com

Surface Roughness

Insertion loss of various copper foils
50 ohm microstrip TL on 0.004" LCP laminate

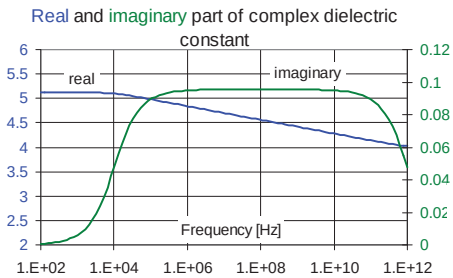


Courtesy of Rogers Corp.

Allen Horn, et.al., "Effect of conductor profile on the insertion loss, phase constant, and dispersion in thin high frequency transmission lines," DesignCon 2010.

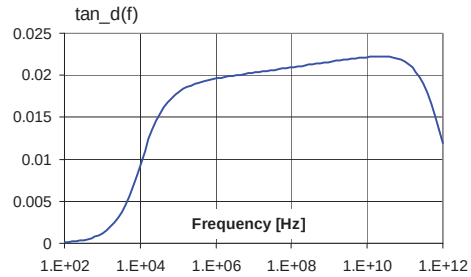
istvan.novak@ieee.org
www.electrical-integrity.com

Dielectric Loss vs. Capacitance



$$\varepsilon_r(f) = \varepsilon_r^{'} - j\varepsilon_r^{''}$$

$$\frac{\varepsilon_r^{''}}{\varepsilon_r} = \tan(\delta)$$



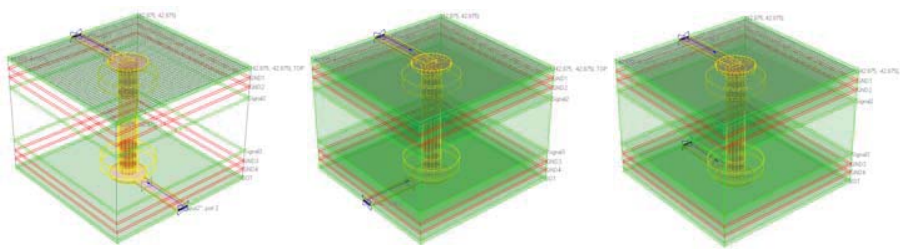
A. Djordjevic, et.al., "Wideband Frequency-Domain Characterization of FR-4 and Time-Domain Causality," IEEE. Tr. EMC, Nov. 2001, p.662

A. Deutsch, et.al., ":Frequency-Dependent Losses on High-Performance Interconnections," IEEE. Tr. EMC, Nov. 2001, p.446

istvan.novak@ieee.org
www.electrical-integrity.com

Via Exit Direction Matters

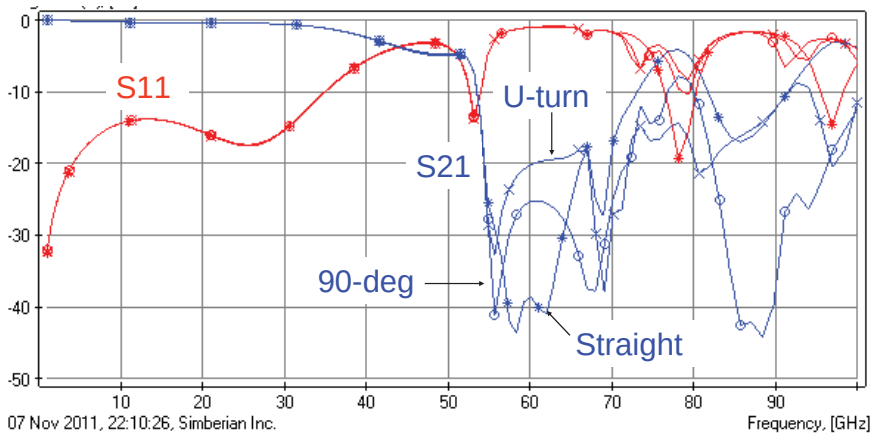
8-layer board, FR4 dielectric, 1ou copper layers, 10-mil drill, 20-mil pad, 30-mil antipad



Bruce Archambeault, et al, "Full Wave Simulation and Validation of a Simple Via Structure," Proceedings of DesignCon 2006, February 6-9, 2006, Santa Clara, CA

istvan.novak@ieee.org
www.electrical-integrity.com

Via Exit Direction Matters

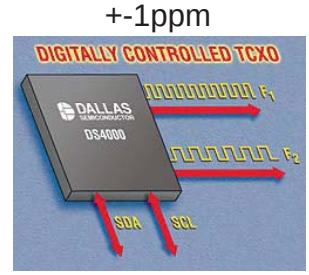


istvan.novak@ieee.org
www.electrical-integrity.com

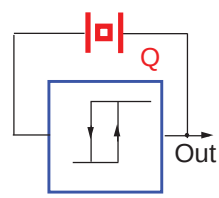
Clock Sources, Selective Timing

- Timing is provided by a selective two pole: quartz crystal or SAW filter or MEMS
- Frequency range up to several hundred MHz
- Narrow tuning range (0.01%)
- Complex circuitry
- Low noise (phase jitter)
- High accuracy and stability
- Less sensitive to stray components and supply noise

+-1ppm



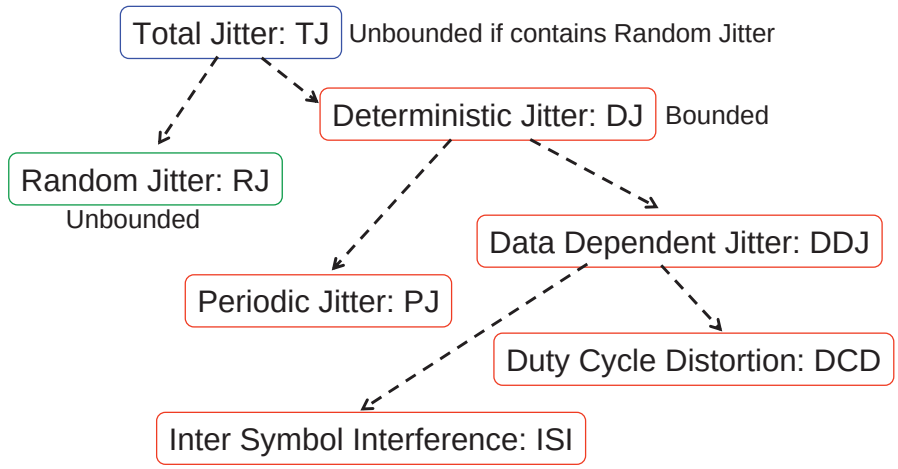
source: http://www.maxim-ic.com



Hysteretic comparator

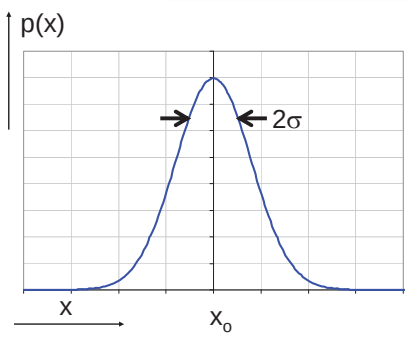
istvan.novak@ieee.org
www.electrical-integrity.com

Decomposition of Jitter



istvan.novak@ieee.org
www.electrical-integrity.com

Random and Total Jitter



x	P(x)
3σ	1.3E-3
4σ	3.2E-5
5σ	2.9E-7
6σ	9.9E-9
7σ	1.3E-12

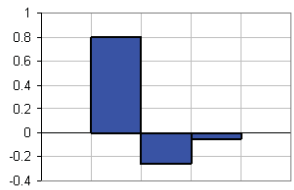
$$p(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(x-x_o)^2}{2\sigma^2}}$$

Total jitter (if it contains RJ) must define bit count

istvan.novak@ieee.org
www.electrical-integrity.com

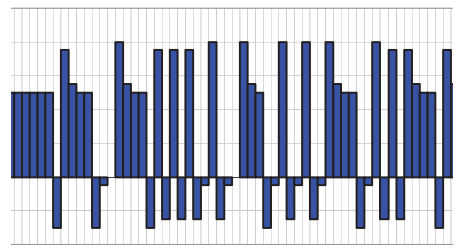
Transmit 6dB Pre-emphasis

FIR filter coefficients



Co = 0.8
C1 = -0.25
C2 = -0.05

Illustrative PRBS pattern with FIR filtering

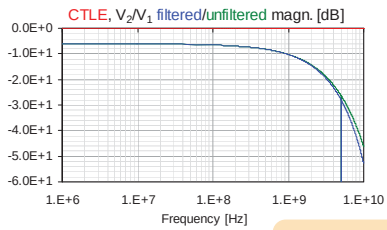


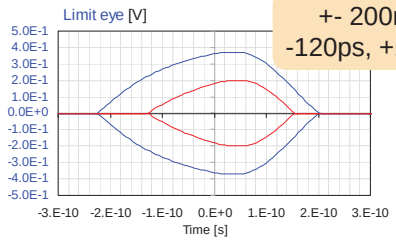
istvan.novak@ieee.org
www.electrical-integrity.com

Receive Equalization, CTLE

Ao	Q
1	0.25
F1	F2
5.0E+08	3.0E+09

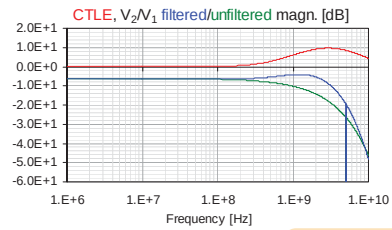
Without CTLE

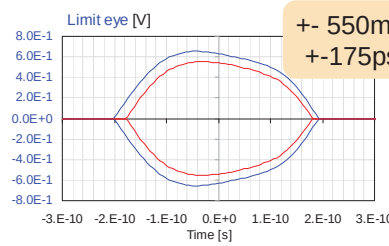




+- 200mV
-120ps, +150ps

With CTLE

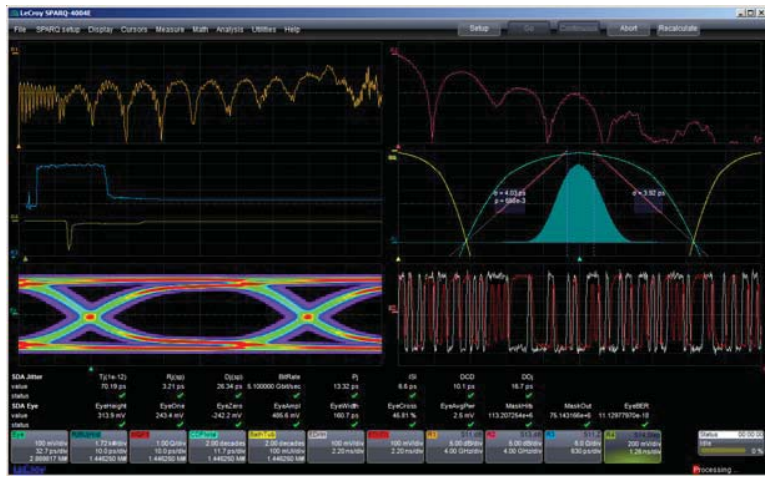




+- 550mV
+-175ps

istvan.novak@ieee.org
www.electrical-integrity.com

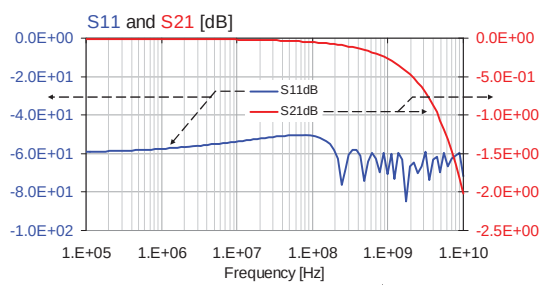
End-to-End Simulation



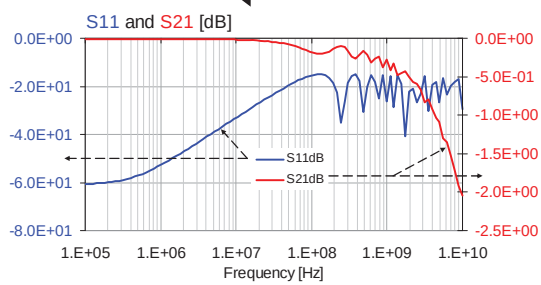
LeCroy
SI Studio

istvan.novak@ieee.org
www.electrical-integrity.com

S Parameters
vs. Normalization impedance



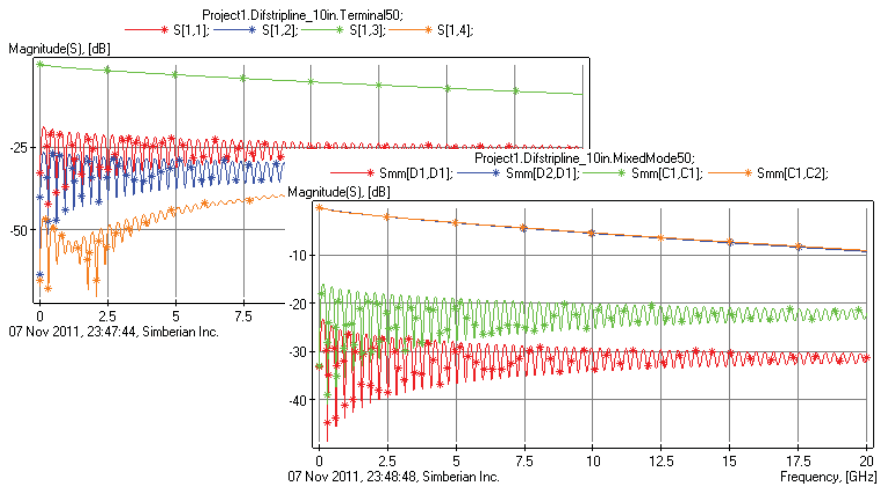
Same 50-ohm trace with 60-ohm normalization



50-ohm trace with 50-ohm normalization

istvan.novak@ieee.org
www.electrical-integrity.com

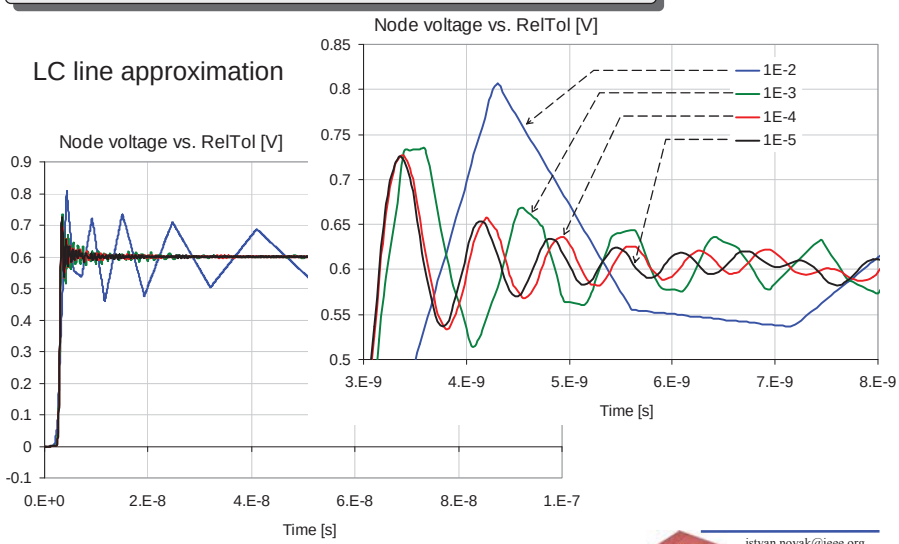
Generalized S Parameters



istvan.novak@ieee.org
www.electrical-integrity.com

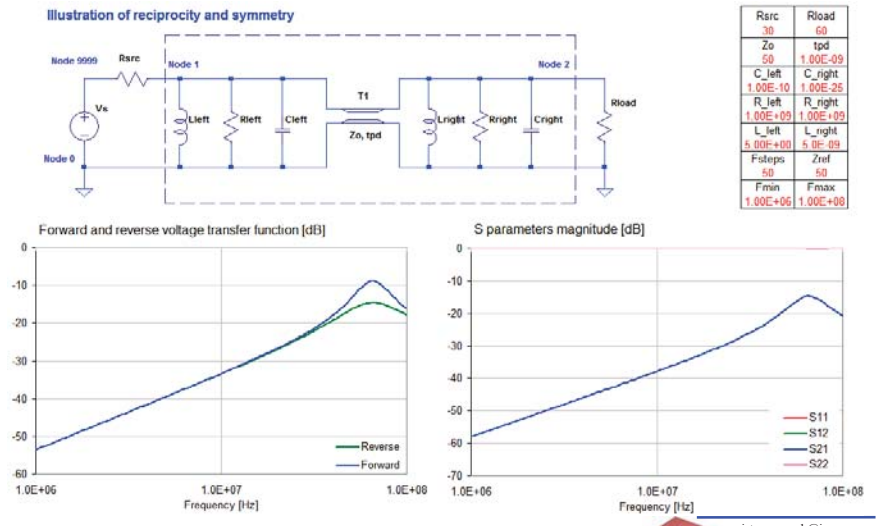
SPICE Parameter Settings

LC line approximation



istvan.novak@ieee.org
www.electrical-integrity.com

Reciprocity and Symmetry: Not the Same



istvan.novak@ieee.org
www.electrical-integrity.com

How to Select Oscilloscopes

Sufficient bandwidth is an absolute must, but alone is not enough.
Look also at:

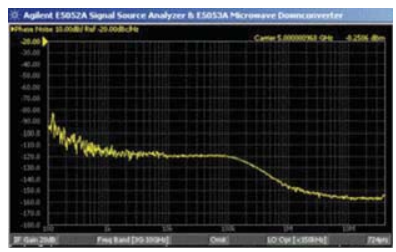
* frequency response curve (group delay)
* sensitivity, noise and jitter floor
* trigger bandwidth and sensitivity
* trigger capability (pulse width, pattern)
* memory depth
* refresh rate
* built-in post-processing
* probe features

Dan Strassberg, "Scopes: More than Meets the Eye," EDN, February 2006

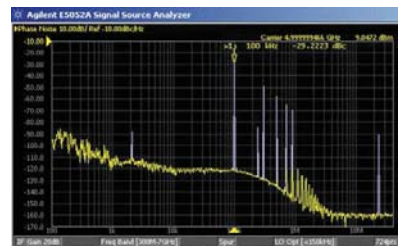
istvan.novak@ieee.org
www.electrical-integrity.com

Measuring Phase Noise vs. Jitter

Random phase noise



Random and periodical phase noise



Phase noise analyzer measures power density.
Periodical jitter in the time domain can not be resolved.

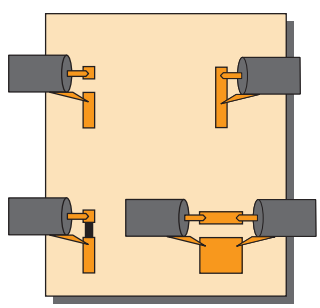
Courtesy, Agilent Technologies, Inc.
Agilent: Using Clock Jitter Analysis to Reduce BER in Serial Data Applications

istvan.novak@ieee.org
www.electrical-integrity.com

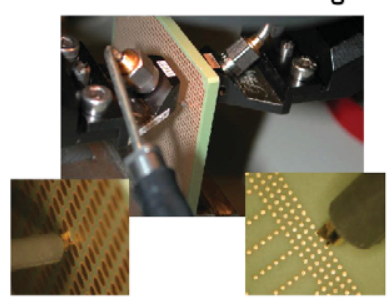
VNA SOLT Calibration

GigaTest Labs

* OPEN
* SHORT
* LOAD
* THROUGH



Two-Sided BGA Probing



Courtesy, GigaTest Labs

* Calibrates to the tip of the wafer probes
* Requires custom calibration substrate

istvan.novak@ieee.org
www.electrical-integrity.com